IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
: Group Art Unit: 2184
M. EROZ et al.)
: Examiner: Not Yet Assigned
Application No: 10/613,824)
:
Filed: July 3, 2003)
:
For: METHOD AND SYSTEM FOR)
   ROUTING IN LOW DENSITY   :   February 26, 2004
   PARITY CHECK (LDPC) DECODERS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56 and in accordance with the practice under 37 C.F.R. §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed Form PTO-1449, and the PCT International Search Report for the corresponding PCT application (PCT/US03/21071). Copies of the documents are enclosed.

FORMAL MATTERS

In accordance with 37 C.F.R. § 1.97(b), an information disclosure statement shall be considered by the Office if filed before the mailing of a first Office action on the merits.   Therefore, it is believed that no fee is required. However, the Commissioner is hereby authorized to charge Deposit Account No. 50-0383 any additional fees which may be deemed to be appropriate or to provide any refunds in connection with this paper to the same Deposit Account. A duplicate of this paper is enclosed.
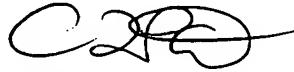
CONCLUSION

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be returned indicating that such information has been considered.

Applicants' undersigned attorney may be reached by telephone at (301) 601-7252. All correspondence should continue to be directed to our address given below.
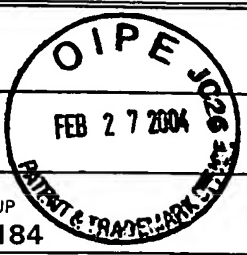
Respectfully submitted,

February 26, 2004

Craig L. Plastrik
Registration No. 41,254

Hughes Electronics Corporation
Customer No. 20991

U.S. DEPARTMENT OF COMMERCE **PATENT AND TRADEMARK OFFICE** LIST OF REFERENCES CITED BY APPLICANT(S) (*Use several sheets if necessary*) Date Submitted to PTO: **February 26, 2004**		ATTY DOCKET NO. **PD-203009**	APPLICATION NO. **10/613,824**				

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APPLICANT **M. EROZ et al.**	
FILING DATE **July 3, 2003**	GROUP **2184**

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		US 2003/0104788	June 5, 2003	Kim	455	67.3	
		US 2003/0074626	April 17, 2003	Coker et al.	714	752	
		US 2003/0023917	January 30, 2003	Richardson et al.	714	749	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO/OR ABSTRACT
		WO 02/103631 A1	December 27, 2002	PCT	G06N	3/00	

OTHER DOCUMENT(S) (Including Author, Title, Data, Pertinent Pages, etc.)

		Mansour et al. , "Low-Power VLSI Decoder Architectures for LDPC Codes", Proceedings, IEEE International Symposium on Lower Power Electronics and Design, ISLPED '02, pp. 284-289, August 12-14, 2002
		T. Zhang et al., "Joint Code and Decoder Design for Implementation-Oriented (3,k)-Regular LDPC Codes", Proceedings, 35th Asilomar Conference on Signals, Systems, & Computers, pp. 1232-1236, November 4-7, 2001
		E. Boutillon et al., "Decoder-First Code Design", Proceedings, International Symposium on Turbo Codes and Related Topics, pp. 459-462, September 4-7, 2000
		G. Al-Rawi et al., "Optimizing the Mapping of Low-Density Parity Check Codes on Parallel Decoding Architectures", Proceedings, IEEE Conference on Information Technology: Coding and Computing, pp. 578-586, April 2-4, 2001
		A. Selvarathinam et al., "A Massively Scaleable Decoder Architecture for Low-Density Parity-Check Codes", Proceedings, IEEE International Symposium on Circuits and Systems, Vol. 2, pp. 61-64, May 25-28, 2003

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

F512\A0000049.DOC (Rev. 4/15/98)

Sheet __1__ of __1__